WHAT IS CLAIMED IS:

1. A reference voltage generating circuit, comprising:

a distributing unit which generates via an output terminal a reference voltage, which has a lower voltage level than that of an external power supply voltage and varies according to an operating mode, in response to the external power supply voltage;

a clamping control unit connected between the output terminal and a ground voltage, the clamping control unit for clamping a voltage level of the reference voltage at a constant level in response to a control voltage having a voltage level which is lower than that of the reference voltage; and

a control unit for increasing or decreasing a voltage level of the reference voltage in response to first and second operating mode signals.

2. The circuit of claim 1, wherein the distributing unit comprises:

a first resistor connected between the external power supply voltage and the output terminal;

a second resistor connected between the output terminal and a first node from which the control voltage is output; and

first through fourth transistors connected in series between the first node and the ground voltage,

wherein the gates of the first through third transistors are connected to the output terminal,

and wherein the external power supply voltage is applied to the gate of the fourth transistor.

3. The circuit of claim 2, wherein the first through fourth transistors are NMOS transistors.

4. The circuit of claim 2, wherein the voltage level of the reference voltage is controlled by controlling a width-to-length ratio of each of the first through fourth transistors.

5. The circuit of claim 2, wherein the control unit comprises:

a first control transistor which is turned on or turned off in response to the first operating mode signal to increase or decrease the reference voltage level; and

a second control transistor which is turned on or turned off in response to the second operating mode signal to increase or decrease the reference voltage level.

6. The circuit of claim 5, wherein the first control transistor is an NMOS transistor, and the source and the drain of the NMOS transistor are connected to the

source and the drain of the first transistor and the first operating mode signal is applied to the gate of the NMOS transistor.

7. The circuit of claim 5, wherein the second control transistor is an NMOS transistor, and the source and the drain of the NMOS transistor are connected to the source and the drain of the third transistor and the second operating mode signal is applied to the gate of the NMOS transistor.

8. The circuit of claim 1, wherein the clamping control unit is a PMOS transistor, and the first and second ends of the PMOS transistor are connected to the output terminal and the ground voltage, respectively, and the control voltage is applied to the gate of the PMOS transistor.

9. The circuit of claim 1, wherein the first and second operating mode signals are mode register set ("MRS") signals.

10. The circuit of claim 1, wherein:

in a low operating frequency range, the first and second operating mode signals are at a first level;

in a high operating frequency range, the first and second operating mode signals are at a second level; and

in an intermediate frequency range, one of the first and second operating mode signals is at the first level and the other is at the second level.

11. An internal voltage generating circuit comprising:

a differential amplifier unit for comparing a voltage level of a reference voltage with a voltage level of an internal voltage to generate a control signal in response to a comparison result and control the voltage level of the internal voltage;

a distributing unit for increasing or decreasing the voltage level of the internal voltage in response to the control signal to clamp the voltage level of the internal voltage at a constant level; and

a control unit for increasing or decreasing the voltage level of the internal voltage in response to a first operating mode signal and a second operating mode signal.

12. The circuit of claim 11, wherein the differential amplifier unit comprises:

a first transistor having a first terminal connected to the external power supply voltage and having the gate and a second terminal, which are connected to each other;

a second transistor having a first terminal connected to the external power supply voltage, the gate connected to the gate of the first transistor, and a second terminal from which the control signal is output;

a third transistor having a first terminal connected to the second terminal of the first transistor, the gate connected to the internal voltage, and a second terminal connected to a first node;

a fourth transistor having a first terminal connected to the second terminal of the second transistor, the gate connected to the reference voltage, and a second terminal connected to the first node; and

a fifth transistor connected between the first node and a ground voltage and having the gate to which a switching signal is applied.

13. The circuit of claim 11, wherein the distributing unit comprises:

a first distributing transistor having a first terminal connected to an external power supply voltage and having the gate to which the control signal is applied;

a second distributing transistor having a first terminal connected to a second terminal of the first distributing transistor and having the gate to which the control signal is applied; and

a third distributing transistor having a first terminal connected to a second terminal of the second distributing transistor, the gate to which the control signal is applied, and a second terminal connected to the internal voltage.

14. The circuit of claim 13, wherein the voltage level of the internal voltage is controlled by controlling a width-to-length ratio of each of the first through third distributing transistors.

15. The circuit of claim 13, wherein the control unit comprises:

a first control transistor which is turned on or turned off in response to the first operating mode signal to increase or decrease the internal voltage level; and

a second control transistor which is turned on or turned off in response to the second operating mode signal to increase or decrease the internal voltage level.

16. The circuit of claim 15, wherein:

the first control transistor is a PMOS transistor, and a first terminal and a second terminal of the first control transistor are respectively connected to the first terminal and second terminal of the second distributing transistor and the first operating mode signal is applied to the gate of the first control transistor; and

the second control transistor is a PMOS transistor, and a first terminal and a second terminal of the second control transistor are respectively connected to the first terminal and the second terminal of the third distributing transistor and the second operating mode signal is applied to the gate of the second control transistor.

17. The circuit of claim 11, wherein the first and second operating mode signals are mode register set ("MRS") signals.

18. The circuit of claim 11, wherein:

in a low operating frequency range, the first and second operating mode signals are at a first level;

in a high operating frequency range, the first and second operating mode signals are at a second level; and

in an intermediate frequency range, one of the first and second operating mode signals is at the first level and the other is at the second level.

19. An internal voltage generating circuit comprising:

a voltage level detecting unit for determining a voltage level of a first voltage in response to first and second operating mode signals to compare the voltage level of the first voltage with a voltage level of a second voltage and control a voltage level of an internal voltage which is higher than a voltage level of an external power supply voltage; and

a boosting unit for increasing or decreasing the voltage level of the internal voltage in response to a control signal, which is generated in response to results of a comparison of the voltage level of the first voltage and the voltage level of the second voltage.

20. The circuit of claim 19, wherein the voltage level detecting unit comprises:

a control unit for receiving a reference voltage to determine the voltage level of the first voltage in response to the first and second operating mode signals; and

a differential amplifier unit for generating the control signal at a first level when the voltage level of the first voltage is higher than that of the second voltage and for generating the control signal at a second level when the voltage level of the first voltage is lower than the second voltage.

21. The circuit of claim 20, wherein the control unit comprises:

first through fourth resistors connected in series between the reference voltage and a ground voltage;

a first control transistor having a first terminal connected between the first resistor and the second resistor, the gate to which the first operating mode signal is applied, and a second terminal connected to a first node between the second resistor and the third resistor; and

a second control transistor having a first terminal connected between the third resistor and the fourth resistor, the gate to which the second operating mode signal is applied, and a second terminal connected between the fourth resistor and the ground voltage.

22. The circuit of claim 21, wherein the first and second operating mode signals are mode register set ("MRS") signals.

23. The circuit of claim 21, wherein:

in a low operating frequency range, the first operating mode signal is at a second level and the second operating mode signal is at a first level; and

in a high operating frequency range, the first operating mode signal is at a first level and the second operating mode signal is at a second level.

24. The circuit of claim 21, wherein the first voltage is a voltage level of the first node.

25. The circuit of claim 20, wherein the differential amplifier unit comprises:

a first transistor having a first terminal connected to the external power supply voltage and having the gate and a second terminal, which are connected to each other;

a second transistor having a first terminal connected to the external power supply voltage, the gate connected to the gate of the first transistor, and a second terminal from which the control signal is output;

a third transistor having a first terminal connected to the second terminal of the first transistor, the gate connected to the first voltage, and a second terminal connected to a second node;

a fourth transistor having a first terminal connected to the second terminal of the second transistor, the gate connected to the second voltage, and a second terminal connected to the first node; and

a fifth transistor connected between the first node and a ground voltage and having the gate to which the external power supply voltage is applied.

26. The circuit of claim 25, wherein the voltage level of the second voltage is proportional to the voltage level of the internal voltage.

27. The circuit of claim 19, wherein the boosting unit is turned on to generate the internal voltage when the control signal is at a first level, and is turned off when the control signal is at a second level.